AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

1. (previously presented) An apparatus for programming non-volatile storage elements, comprising:

a programming circuit in communication with said non-volatile storage elements;

a common control line connected to said non-volatile storage elements and in communication with said programming circuit; and

one or more verification selection circuits in communication with said non-volatile storage elements, said one or more verification selection circuits cause a first subset of said non-volatile storage elements connected to said common control line to be subjected to coarse verification concurrently while a second subset of said non-volatile storage elements connected to said common control line are subjected to fine verification.

2. (cancelled)

3. (original) An apparatus according to claim 1, wherein:

said one or more verification selection circuits include one verification selection circuit for each non-volatile storage element of a subset of non-volatile storage elements.

4. (original) An apparatus according to claim 1, wherein at least one of said one or more verification selection circuits comprises:

a sense circuit in communication with a first non-volatile storage element;

a programming mode indication circuit, in communication with said sense circuit, providing an output indicating whether said first non-volatile storage element is in a coarse programming mode or a fine programming mode based on said sense circuit; and

a selection circuit in communication with said programming mode indication circuit, said selection circuit applies a coarse verification signal to said first non-volatile storage element if said first non-volatile storage element is in said coarse programming mode and applies a fine verification signal to said first non-volatile storage element if said first non-volatile storage element is in said fine programming mode.

5. (previously presented) An apparatus according to claim 1, wherein at least one of said one or more verification selection circuits comprises:

a storage unit, said storage unit storing data indicating whether a first non-volatile storage element is in a coarse programming mode or a fine programming mode;

a first switch in communication with said first non-volatile storage element;

sense circuit connected to said first switch and providing an output to said storage unit, said storage unit uses said output from said sense circuit to indicate whether said first non-volatile storage element is in said coarse programming mode or said fine programming mode; and

a second switch in communication with said storage unit and having an output connected to said sense circuit, said second switch receiving a coarse reference signal and a fine reference signal and providing either said coarse reference signal or said fine reference signal at said output of said second switch in response to said storage unit.

6. (original) An apparatus according to claim 5, wherein:

said non-volatile storage elements are flash memory devices.

7. (original) An apparatus according to claim 5, wherein:

said coarse reference signal and said fine reference signal provide reference currents.

8. (original) An apparatus according to claim 5, wherein:

said coarse reference signal and said fine reference signal provide reference voltages.

9. (original) An apparatus according to claim 5, wherein:

said coarse reference signal and said fine reference signal provide an indication of discharge times.

10. (original) An apparatus according to claim 1, wherein:

said coarse verification and said fine verification are performed using a discharge method.

11. (original) An apparatus according to claim 1, wherein:

said programming circuit includes a controller and a state machine; and

said programming circuit is separate from said one or more verification selection circuits.

12. (original) An apparatus according to claim 1, wherein:

said non-volatile storage elements are multi-state flash memory devices.

13. – 23. (cancelled)

24. (cancelled)

25. (currently amended) A method ~~according to claim 24, wherein:~~ for programming non-volatile storage elements, comprising:

providing a common programming signal to said non-volatile storage elements, said step of providing is part of a programming process that includes a coarse programming phase and a fine programming phase such that one or more of said non-volatile storage elements are in said coarse programming phase while one or more of said non-volatile storage elements are in said fine programming phase, said step of providing includes providing said common programming signal to a word line common to at least a subset of said one or more of said non-volatile storage elements that are in said coarse programming phase and said one or more of said non-volatile storage elements that are in said fine programming phase; and

performing coarse verification for said one or more of said non-volatile storage elements that are in said coarse programming phase while concurrently performing fine verification for said one or more of said non-volatile storage elements that are in said fine programming phase.

26. (currently amended) A method according to claim ~~24,~~ 47, wherein:

said set of non-volatile storage elements are flash memory devices.

27. (currently amended) A method according to claim ~~24,~~ 47, wherein:

said set of non-volatile storage elements are multi-state flash memory devices.

28. (currently amended) A method according to claim ~~24,~~ 47, further comprising:

using said coarse verification to determine when a particular non-volatile storage element completes said coarse programming phase and ~~causing~~ cause said particular non-volatile storage element to begin said fine programming phase.

29. (original) A method according to claim 28, wherein:

following said non-volatile storage element beginning said fine programming phase, said non-volatile storage element begins said fine verification.

30. (original) A method according to claim 28, wherein:

causing said particular non-volatile storage element to begin said fine programming phase includes raising a bit line voltage.

31. (original) A method according to claim 28, wherein said step of performing comprises:

performing coarse verification for said particular non-volatile storage element without performing fine verification for said particular non-volatile storage element, if said particular non-volatile storage element is determined to be in said coarse programming phase; and

performing fine verification for said particular non-volatile storage element without performing coarse verification for said particular non-volatile storage element, if said particular non-volatile storage element is determined to be in said fine programming phase.

32. (currently amended) A method according to claim ~~24,~~ 47, wherein:

said coarse verification and said fine verification are based on a bit line discharge process.

33. (currently amended) A method according to claim ~~24~~ 25, wherein said step of performing comprises:

pre-charging a first bit line based on a coarse pre-charge signal if a first non-volatile storage element is in said coarse programming phase;

pre-charging said first bit line based on a fine pre-charge signal if said first non-volatile storage element is in said fine programming phase;

applying a verify signal to a control gate for said first non-volatile storage element; and

allowing said bit line to discharge for a fixed period of time.

34. (currently amended) A method according to claim ~~24~~ 25, wherein said step of performing comprises:

pre-charging a first bit line for a first non-volatile storage element;

applying a verify signal to a control gate for said first non-volatile storage element;

determining a time for said bit line to discharge until a voltage or a current of said bit line reaches a predetermined value;

comparing a coarse compare value to said time, if said first non-volatile storage element is in said coarse programming phase; and

comparing a fine compare value to said time, if said first non-volatile storage element is in said fine programming phase.

35. (original) A method according to claim 34, wherein:

said predetermined value is a first value if said first non-volatile storage element is in said coarse programming phase; and

said predetermined value is a second value if said first non-volatile storage element is in said fine programming phase.

36. – 39. (cancelled)

40. (currently amended) A method according to claim ~~24~~ 25, wherein:

said step of providing includes providing said common programming signal to steering gates.

41. (currently amended) A method ~~according to claim 24, wherein:~~ for programming non-volatile storage elements, comprising:

providing a common programming signal to said non-volatile storage elements, said non-volatile storage elements are connected to a common control line, said step of providing is part of a programming process that includes a coarse programming phase and a fine programming phase such that one or more of said non-volatile storage elements are in said coarse programming phase while one or more of said non-volatile storage elements are in said fine programming phase; and

performing coarse verification for said one or more of said non-volatile storage elements that are in said coarse programming phase while concurrently performing fine verification for said one or more of said non-volatile storage elements that are in said fine programming phase.

42. (currently amended) A method according to claim ~~24,~~ 47, wherein:

said set of non-volatile storage elements are connected to a common word line.

43. (previously presented) An apparatus according to claim 1, wherein:

said common control line is a word line..

44. (cancelled)

45. (previously presented) An apparatus for programming non-volatile storage elements, comprising:

a programming circuit in communication with said non-volatile storage elements, said programming circuit programs said non-volatile storage elements together as part of a common coarse/fine programming process; and

one or more verification selection circuits in communication with said non-volatile storage elements, said one or more verification selection circuits cause a first subset of said non-volatile storage elements to be subjected to coarse verification concurrently while a second subset of said non-volatile storage elements are subjected to fine verification.

46. (previously presented) An apparatus for programming non-volatile storage elements, comprising:

an array of non-volatile storage elements;

a programming circuit in communication with said array of non-volatile storage elements, said programming circuit programs said array of non-volatile storage elements using a coarse/fine programming process; and

one or more verification selection circuits in communication with said array of non-volatile storage elements, said one or more verification selection circuits cause a first subset of said array of non-volatile storage elements to be subjected to coarse verification concurrently while a second subset of said array of non-volatile storage elements are subjected to fine verification.

47. (previously presented) A method for programming non-volatile storage elements, comprising:

providing a programming signal to a set of non-volatile storage elements being programmed together as part of a common coarse/fine programming process that includes a coarse programming phase and a fine programming phase such that one or more of said non-

volatile storage elements are in said coarse programming phase while one or more of said non-volatile storage elements are in said fine programming phase; and

performing coarse verification for said one or more of said non-volatile storage elements that are in said coarse programming phase while concurrently performing fine verification for said one or more of said non-volatile storage elements that are in said fine programming phase.